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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

REPLY BRIEF FOR THE APPELLANT

Ex parte Olav TIRKKONEN et al.

POWER ALLOCATION IN A COMMUNICATION SYSTEM

Serial No. 10/632,089
Appeal No.: Unknown
Group Art Unit: 2618

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Enclosure: Reply Brief

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Appellant:	Confirmation No.: 3395
Olav TIRKKONEN et al.	Appeal No.: Unknown
Serial Number: 10/632,089	Group Art Unit: 2618
Filed: August 1, 200o3	Examiner: Duc M. Nguyen

For: POWER ALLOCATION IN A COMMUNICTION SYSTEM

REPLY BRIEF

August 27, 2007

I. INTRODUCTION

This Reply Brief is filed in response to the Examiner's Answer dated June 25, 2007. In that Examiner's Answer, while no new grounds of rejection are made, comments and explanations are provided which are tantamount to new points of argument. This Reply Brief, therefore, is submitted to address these new points of argument, and to clarify why claims 1-23 of the pending application should be considered to be patentable over Sadjadpour et al. (U.S. Publication No. 2001/0055332), Applicants' admitted prior art (AAPA) and Kim et al. (U.S. Publication No. 2003/0128769), and, therefore, should be found by this Honorable Board of Patent Appeals and Interferences to be allowable.

This Reply Brief addresses a few of the deficiencies of the Examiner's Answer. Appellant's Appeal Brief, however, is maintained, and failure to repeat the arguments

contained therein, or to address one or more argument set forth in the Examiner's Answer should not be construed as waiver or an admission. The Appeal Brief speaks for itself, and this Reply Brief merely supplements the Appeal Brief to address certain aspects of the Examiner's Answer.

II. STATUS OF CLAIMS

Claims 1-23 all of the claims pending in the present application, are the subject of this appeal. Claims 1, 18, and 23 were rejected under 35 USC 102(a) as being anticipated by Sadjadpour (U.S. Patent Publication No. 2001/0055332). Claims 2-13, 19, 20, and 22 were rejected under 35 USC 102(a) as being unpatentable over Sadjadpour, in view of Applicants' admitted prior art (AAPA). Claims 14-17, and 21 were rejected under 35 USC 103(a) as being obvious over Sadjadpour, in view of AAPA, and further in view of Kim (U.S. Patent Publication No. 2003/0128769).

III. APPELLANT'S ARGUMENTS

Appellants respectfully submit that each of pending claims 1-23 recites subject matter that is not taught, disclosed, or suggested by Sadjadpour, AAPA, and Kim. As discussed in Appellant's Appeal Brief, Sadjadpour does not teach or suggest "circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate" and "circuitry configured to select a bit loading sequence with a lowest error rate," as recited in claim 1. Similarly, Sadjadpour does not teach or suggest

"determining a power allocation for at least one bit loading sequence based on minimizing an error rate" and "selecting a bit loading sequence with a lowest error rate and applying the power allocation to at least one communication channel," as recited in claim 18. Sadjadpour also does not teach or suggest "determining means for determining a power allocation for at least one bit loading sequence based on minimizing an error rate" and "selecting means for selecting a bit loading sequence with a lowest error rate," as recited in claim 23.

In the Examiner's Answer, the Examiner appears to take the position that blocks 61-68, illustrated in Figure 6 of Sadjadpour, anticipate the above-recited limitations of the present claims. In particular, the Examiner's Answer cited block 62 of Sadjadpour as being a function that determines a power allocation for at least one bit loading sequence based on minimizing an error rate. Appellants respectfully disagree. Sadjadpour discloses that "function 62 represents joint minimization of the Bit Error Rate (BER) and maximization of the total data rate" (Sadjadpour, paragraph 0044). Thus, function 62 minimizes the average BER while still maximizing the total data rate (Sadjadpour, Figure 6). In other words, function 62 of Sadjadpour does not absolutely minimize the BER since it must also maximize the total data rate. Accordingly, Sadjadpour fails to disclose or suggest determining a power allocation for at least one bit loading sequence based on minimizing an error rate and selecting a bit loading sequence with a lowest error rate.

Appellants submit that the other functions of Sadjadpour cited by the final Office Action and Examiner's Answer also do not anticipate the above-recited limitations of the claims. Function 64 represents the joint minimization of an arbitrary function of the total

power and maximization of the total data rate such as would be achieved using the algorithm described in paragraphs 0036-0038. Similarly, function block 61 shows the functions which apply joint minimization of the cross talk and maximization of the total data rate, as is shown in the method described in paragraphs 0039-0042. Therefore, Sadjadpour only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. Sadjadpour fails to disclose or suggest selecting a bit loading sequence with the lowest error rate.

Thus, Sadjadpour does not disclose or suggest "circuitry configured to determine a power allocation for at least one bit loading sequence based on minimizing an error rate" and "circuitry configured to select a bit loading sequence with a lowest error rate," as recited in claim 1, and the similar limitations recited in claims 18 and 23.

Claims 2-13, 19, 20, and 22 stand rejected under 35 U.S.C. §103(a) as being obvious in view of Sadjadpour in view of Applicants' admitted prior art (Fig. 1-2 and [0005]-[0023], hereafter, AAPA).

Claims 2-13 are dependent upon claim 1 and recite further limitations. Thus, Appellants submit that claims 2-13 are patentable at least for the reasons claim 1 is patentable, and further, because they recite additional limitations.

With respect to claim 19, Sadjadpour does not teach or suggest "a third circuitry for choosing a bit loading sequence having a minimum error rate." As discussed in the Appeal Brief, Sadjadpour only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and

minimizing cross talk. Additionally, Sadjadpour discloses a function 62 which does not absolutely minimize the BER since it must also maximize the total data rate. Sadjadpour, therefore, fails to disclose or suggest third circuitry for choosing a bit loading sequence having a minimum bit error rate. Appellants respectfully submit that there is simply no disclosure or suggestion in Sadjadpour of any elements which could be comparable to the third circuitry as recited in claim 19, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate.

Further, Appellants submit that the cited portions of Appellants' specification (paragraphs [0005]-[0023]) also do not teach, show, or suggest "a third circuitry for choosing a bit loading sequence having a minimum error rate," as recited in claim 19. As such, Appellants submit that AAPA does not further the teaching of Sadjadpour to the level necessary to properly support an obviousness rejection of claim 19.

The combination of Sadjadpour and AAPA fails to disclose or suggest all of the elements of claim 19. Therefore, reconsideration and withdrawal of the rejection of these claims is respectfully requested.

With respect to claim 10, Appellants submit that Sadjadpour does not teach or disclose allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate, as recited in claim 20. The Examiner's Answer asserted that the sub-bands of QAM channels in Sadjadpour, or the independent sub-channels in AAPA read on the claimed "logical channels," while the "weighted

combination" in Sadjadpour or the "weighing unit" in AAPA read on the claimed "power weighting."

However, as discussed above, Sadjadpour only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. Sadjadpour, however, fails to disclose or suggest allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences and choosing a bit loading sequence having a minimum bit error rate. Appellants respectfully submit that there is simply no disclosure or suggestion in Sadjadpour of any elements which could be comparable to the allocating and choosing steps recited in claim 20, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate.

Further, Appellants submit that the cited portions of Appellants' specification (paragraphs [0005]-[0023]) also do not teach, show, or suggest the limitations recited in claim 20. More particularly, Appellants submit that AAPA does not teach allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate. As such, Appellants submit that AAPA does not further the teaching of Sadjadpour to the level necessary to properly support an obviousness rejection of claim 20.

Appellants, therefore, respectfully assert that the combination of Sadjadpour and AAPA does not disclose or suggest all of the elements of claim 20. Thus, reconsideration and withdrawal of the rejection of claim 20 is respectfully requested.

With respect to claim 22, Sadjadpour does not teach or disclose allocating means for allocating a power weighting to the corresponding logical channels for minimizing a bit error rate of the identified bit loading sequences and choosing means for choosing a bit loading sequence having a minimum bit error rate, as recited in claim 22. As discussed above, Sadjadpour only discloses selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk. Sadjadpour, however, fails to disclose or suggest allocating a power weighting to the corresponding logical channel for minimizing a bit error rate of corresponding bit loading sequences from the set of bit loading sequences and choosing a bit loading sequence having a minimum bit error rate. Function 62 of Sadjadpour is directed to minimizing the average BER while still maximizing the total data rate (Sadjadpour, Figure 6). In other words, function 62 of Sadjadpour does not absolutely minimize the BER since it must also maximize the total data rate.

Further, Appellants submit that the cited portions of Appellants' specification (paragraphs [0005]-[0023]) also do not teach, show, or suggest the limitations recited in claim 20. More particularly, Appellants submit that AAPA does not teach allocating power weighting to a logical channel for minimizing a bit error rate of a corresponding bit loading sequence and choosing at least one bit loading sequence based on minimizing an error rate. As such, Appellants submit that AAPA does not further the teaching of

Sadjadpour to the level necessary to properly support an obviousness rejection of claim 22.

Appellants, therefore, respectfully assert that the combination of *Sadjadpour* and AAPA does not disclose or suggest all of the elements of claim 22. Thus, reconsideration and withdrawal of the rejection of claim 22 is respectfully requested.

Additionally, in response to Appellants arguments that the cited references are not properly combinable, the Examiner's Answer asserted "since Sadjadpour and AAPA both directed to a communication device (i.e, a phone), a bit and power allocation algorithm (voice coding), and since one skilled in the art would recognize that the voice coding (or bit and power allocation) algorithm would apply and work equally well for both wired phones and wireless phones, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Sadjadpour's teaching to a wireless system for reducing cross-talk in wireless phone as well" (Examiner's Answer, page 14). Appellants submit that the Examiner's Answer has concluded that "the voice coding (or bit and power allocation) algorithm would apply and work equally well for both wired phones and wireless phones," without providing any support for such a conclusion.

Furthermore, Appellants note that the method shown in the description of Sadjadpour is specifically related to the problem of cross talk in twisted pair modems, and as such, the method of Sadjadpour describes a weighting algorithm to reduce cross talk based on twisted pair cross talk algorithms. Even if a person of skill in the art were to examine the teaching of Sadjadpour, they would not have considered Sadjadpour to be a suitable starting point for generating Appellants' claimed invention. Appellants submit

that the cited references do not include any motivation or suggestion for applying Sadjadpour's method to a wireless environment. Thus, Appellants submit that in the absence of any teaching, suggestion, or motivation to do so found in the references themselves, a person skilled in the art would not have considered modifying a twisted pair modem communication technique for application in a wireless communication system, and combination of such teachings is inappropriate. Thus, Appellants submit that the references cited in support of the §103 rejection are not properly combined, and reconsideration and withdrawal of the obviousness rejections is respectfully requested.

Claims 14-17 and 21 were rejected under 35 U.S.C. §103(a) as being obvious in view of *Sadjadpour* in view of AAPA, further in view of *Kim* (U.S. Publication No. 2003/0128769).

Claims 14-17 and 21 are dependent upon claims 1 and 20, respectively, and recite additional limitations. Thus, Appellants submit that claims 14-17 and 21 are patentable at least for the reasons claims 1 and 20 are patentable, and further, because they recite additional limitations.

V. CONCLUSION

As explained above and in the Appeal Brief, each of claims 1-23 recites subject matter which is neither disclosed nor suggested by the cited art of Sadjadpour, AAPA and Kim. As such, Appellants submit that the final Office Action has failed to establish a prima facie case for anticipation or obviousness. Since the final rejection is in error, it is

respectfully requested that this honorable Board of Patent Appeals and Interferences reverse the Examiner's decision in this case and indicate the allowability of claims 1-23.

In the event that this paper is not being timely filed, the applicant respectfully petitions for any appropriate extension of time. Any fees for such an extension together with any additional fees which may be due with respect to this paper may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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